Thomas Mikolajick, Stefan Slesazeck, Min Hyuk Park, Uwe Schroeder

Ferroelectric hafnium oxide for ferroelectric random-access memories and ferroelectric field-effect transistors

Erstveröffentlichung in / First published in:

MRS bulletin. 2018, 43 (5), S. 340– 346 [Zugriff am: 15.04.2020]. Cambridge University Press. ISSN 1938-1425.

DOI: https://doi.org/10.1557/mrs.2018.92

Ferroelectric hafnium oxide for ferroelectric random-access memories and ferroelectric field-effect transistors

Thomas Mikolajick, Stefan Slesazeck, Min Hyuk Park, and Uwe Schroeder

Ferroelectrics are promising for nonvolatile memories. However, the difficulty of fabricating ferroelectric layers and integrating them into complementary metal oxide semiconductor (CMOS) devices has hindered rapid scaling. Hafnium oxide is a standard material available in CMOS processes. Ferroelectricity in Si-doped hafnia was first reported in 2011, and this has revived interest in using ferroelectric memories for various applications. Ferroelectric hafnia with matured atomic layer deposition techniques is compatible with three-dimensional capacitors and can solve the scaling limitations in 1-transistor-1-capacitor (1T-1C) ferroelectric random-access memories (FeRAMs). For ferroelectric field-effect-transistors (FeFETs), the low permittivity and high coercive field E_c of hafnia ferroelectrics are beneficial. The much higher E_c of ferroelectric hafnia, however, makes high endurance a challenge. This article summarizes the current status of ferroelectricity in hafnia and explains how major issues of 1T-1C FeRAMs and FeFETs can be solved using this material system.

Introduction

Ferroelectric materials have two nonzero spontaneous polarization states in the absence of an applied electric field. The most frequently used ferroelectric material class are perovskites with the general structure of ABO_3, where A and B are cations (e.g., $BaTiO_3$ [BTO] and $PbZr_xTi_{1-x}O_3$ [PZT]). In PZT, the B site can be occupied by either a titanium cation or zirconium cation. Perovskites typically undergo a phase transition from a nonferroelectric cubic phase at higher temperatures to a ferroelectric tetragonal phase at lower temperatures. **Figure 1**a shows a PZT crystal in the tetragonal phase. It becomes clear that the smaller cation (Ti^{4+} or Zr^{4+}) can have two stable positions resulting in two opposite polarization states. The blue and the green cations in Figure 1 indicate the two stable positions. Please note that the Ti^{4+} or the Zr^{4+} will occupy one of the two positions only. Therefore, the polarization of ferroelectrics can be reversed when an external electrical field greater than the coercive field E_c is applied[1] (Figure 1a–d). Since the polarization reversal process is purely field driven, without a sufficient applied field, the polarization will remain in the previously set direction; therefore, ferroelectricity is ideal for low-power binary nonvolatile memory having two stable states that represent "0" and "1" data (Figure 1b–c). All other known emerging nonvolatile memory concepts, such as spin torque transfer magnetic random-access memory or resistive random-access memory, require passing a current through the device. Consequently, there is limited efficiency in the writing process, since not every electron that passes through the structure will contribute to the switching effect.[2] The field-driven polarization reversal thus gives ferroelectrics a unique selling point for nonvolatile memories.

As early as 1952,[3,4] the first attempts were made to realize memories based on the ferroelectric effect in barium titanate crystals. However, to mitigate problematic issues caused by the voltages applied to currently unselected cells that are connected to the same wordline or bitline of the active cells, researchers found that a selector device, which will only be turned on if the cell is operated, needed to be added. This possibility only became available after semiconductor technology reached a certain level of maturity in the 1970s and 1980s. The resulting "1 transistor—1 ferroelectric capacitor" memory (see **Figure 2**a) reached the market in the early 1990s.[5] This success

Thomas Mikolajick, TU Dresden, Germany; and Nanoelectronic Materials Laboratory GmbH, Germany; thomas.mikolajick@namlab.com
Stefan Slesazeck, Nanoelectronic Materials Laboratory gGmbH, Germany; stefan.slesazeck@namlab.com
Min Hyuk Park, Nanoelectronic Materials Laboratory gGmbH, Germany; minhyuk.park@namlab.com
Uwe Schroeder, Nanoelectronic Materials Laboratory gGmbH, Germany; uwe.schroeder@namlab.com
doi:10.1557/mrs.2018.92

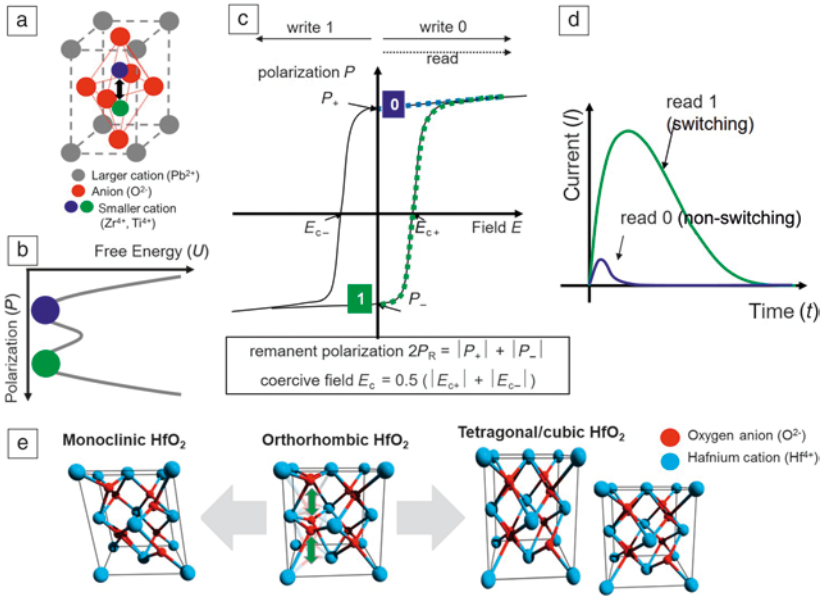


Figure 1. (a) Perovskite crystal illustrating the two potential stable positions (blue and green circles) of a central cation (e.g., Ti^{4+} or Zr^{4+} in $Pb(Zr, Ti)O_3$). (b) Corresponding diagram of the free energy, *U*, as a function of the polarization, *P*. (c) Resulting polarization, *P*, as a function of the electrical field, *E*, for a ferroelectric capacitor indicating the pulses that need to be applied for writing and reading. The green and blue color of the hysteresis in (c) correspond to the blue and green positions of the central cation, as shown in the (a) perovskite crystal. (d) When the reading pulses are applied, a current will flow according to the previously stored state. (e) Different crystal structures detected in thin hafnium oxide films. The orthorhombic structure can be observed under conditions that are typically located between those that establish the tetragonal/cubic phase and the monoclinic phase. The green arrows indicate the possible movements of the oxygen ions between the two possible stable configurations. Note: E_{c+}, positive coercive field; E_{c-}, negative coercive field; P_+, positive remanent polarization; P_-, negative remanent polarization.

inspired the industry, and by the end of the 1990s and early 2000s, all major memory companies had programs to develop ferroelectric random-access memories (FeRAMs). The primary aim was to achieve a device that would have similar performance and cell size to dynamic random-access memories (DRAMs), yet, at the same time, be nonvolatile. Despite some significant advances,[6,7] this goal could not be reached since scaling down the cell size was hindered by integration issues, such as high thermal budget, hydrogen sensitivity, and the unavailability of advanced deposition techniques, of the complex perovskite or layered perovskite ferroelectrics. Ultimately, the required three-dimensional (3D) integration of the capacitor became an unsolvable issue[8,9] (until the present). The technology stalled at the 130-nm process generation[10] and did not follow the scaling of other technologies into the 20-nm regime available today. Therefore, the cost per bit remains high, and the technology remained limited to niche applications where the low-power write operation was an absolute must. The resulting high cost was accepted due to the absence of alternatives.

Early on, another path seemed attractive. In the FeRAM described so far, a ferroelectric capacitor is used as the storage device and reading of the stored information is performed by evaluating the current response due to switching (or not switching) the capacitor with an applied voltage (see Figure 1d). The ferroelectric can instead be integrated into the gate stack of a ferroelectric field-effect transistor (FeFET) (**Figure 3**).[11] The current in the device is modulated based on the polarization of the ferroelectric layer. However, this solution had additional issues. Since perovskites have a high permittivity (in the range of a few hundreds), the series connection between the ferroelectric, the interface oxide, and the depletion layer in the silicon leads to a depolarization field across the ferroelectric in the retention case were no external voltage is applied, making nonvolatility difficult to achieve.[12]

After four decades of research, nonvolatile FeFETs were demonstrated using $SrBi_2Ta_2O_9$ (SBT). However, to achieve a reasonable memory window and mitigate the depolarization issue, a thick ferroelectric needed to be used, defeating the purpose of better scalability.[13] Therefore, in the time frame from approximately 2005 to 2011, it seemed that the physical advantage of ferroelectrics for nonvolatile storage would remain restricted to niche applications such as data logging where frequent overwrites are required. Industry attention turned to other concepts based on resistive change such as magnetoresistive memories, phase-change memories, valence-change memories, or electrochemical metallization memories. It was clear that the main issue was the complexity of the ferroelectric materials (such as the one shown in Figure 1a) that could only be overcome in complementary metal oxide semiconductor (CMOS) processing under severe limitations, such as integrating oxide electrodes to solve reliability issues and hydrogen barrier layers to protect the ferroelectric from the effects of hydrogen exposure during further processing.

Ferroelectricity in hafnium oxide

In the late 1990s, hafnium oxide became one of the most prominent high-*k* (*k* represents the dielectric constant or permittivity) materials to replace the well-established silicon dioxide in metal oxide semiconductor field-effect transistors. Hafnium oxide has reasonably high permittivity and bandgap, and is stable on silicon.[14] In terms of minimum leakage, the amorphous phase was preferred in transistors that became available in 2007.[15] However, crystalline phases of HfO_2 (see Figure 1e) have higher permittivity than the amorphous phase. Among these, the monoclinic (space group: $P2_1/c$), the tetragonal (space group: $P4_2/nmc$), and the cubic (space group: $Fm\bar{3}m$) phases can be formed under reasonable conditions. They have permittivities of 22, 46, and 36, respectively (Figure 1e).[16] In bulk material, the monoclinic phase is the stable phase at room

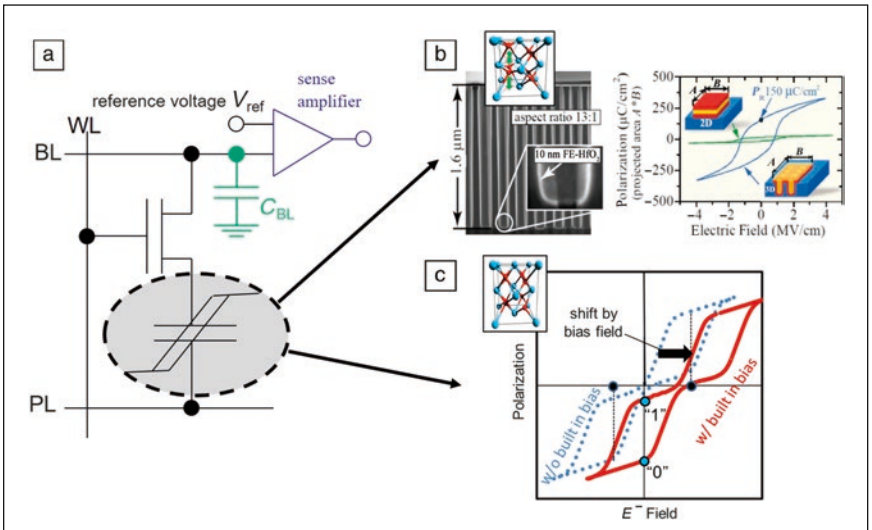


Figure 2. Realization of nonvolatile random-access memories (RAMs) using ferroelectric and antiferroelectric hafnium oxide. (a) Circuit diagram of conventional ferroelectric random-access memory (FeRAM), using (b) ferroelectric hafnium oxide to overcome the 3D integration challenge. (Left) Transmission electron microscope image of the cross section of 10-nm aluminum-doped hafnium oxide in a 3D structure; (right) hysteresis for the 3D structure (blue) and a planar structure having the same projected area *A*B* (green). The orthorhombic hafnium oxide structure in the inset of the left figure indicates the required crystal phase and is explained in Figure 1e. (b) Reprinted with permission from IEEE.[68] (c) Antiferroelectric memory concept to overcome the limitations in cycle endurance and low-voltage operation. The dotted hysteresis loop shows the original antiferroelectric hysteresis. The solid hysteresis loop shows the hysteresis after it was shifted by a built-in voltage using electrodes with different work functions. The circles marked "0" and "1" on the solid hysteresis loop indicate the two states used for information storage. The tetragonal hafnium oxide structure in the inset indicates the required crystal phase and is explained in Figure 1e. Red spheres represent oxygen anions, and blue spheres represent hafnium cations; green arrows indicate the possible movements of the oxygen ions between the two possible stable configurations. Note: FE, ferroelectric; BL, bit line; WL, word line; PL, plate line; C_{BL}, bit-line capacity; P_R, remanent polarization.

temperature and 1 atm, and it transforms to the tetragonal and cubic phase at 1973 and 2773 K, respectively.

The tetragonal or cubic phase induced by doping in hafnium oxide has been studied intensively. Boescke first observed a clear fingerprint of ferroelectricity in silicon doped hafnium oxide samples with doping concentrations in the few percent range.[17,18] Since this discovery was unexpected, researchers initially used different evaluation techniques to experimentally prove that the ferroelectric hysteresis does not originate from artifacts such as leakage[19] or charge trapping. Piezoelectricity[20] and pyroelectricity[21,22] have been demonstrated as well. Additionally, it was shown that different dopants such as Si,[17] Y,[23] Al,[24] Zr,[25] and others[26,27] can induce ferroelectricity. Even in undoped HfO_2,[28] it is possible to achieve ferroelectricity by further reducing the film thickness and choosing proper processing conditions. From the beginning, it was speculated that the noncentrosymmetric orthorhombic $Pca2_1$ phase could be responsible for this behavior.[17,18]

However, with standard methods such as x-ray diffraction, a bulletproof verification of the orthorhombic phase in a mixture of monoclinic and tetragonal phases could not be achieved. Sang et al.[29] used position averaged convergent beam electron diffraction analysis to prove that the orthorhombic $Pca2_1$ phase is present in ferroelectric hafnium oxide. Using this knowledge in modeling makes identification of phase fractions more convenient.[30] Nonetheless, the factors leading to the formation of the orthorhombic phase are still not clear. Many factors such as stress, grain size, and doping may play a role. Materlik et al.[16] proposed that surface energy can be the most important factor, based on the fact that the gain in free energy of these factors is not sufficient to explain the stabilization of the orthorhombic phase and why the stabilization works much better in thinner films.[31] Park et al.[32] recently compared this model to experimental data in hafnium zirconium oxide. It was found that the basic experimental trends with respect to film composition confirm the model, but the best composition to achieve ferroelectric behavior is shifted to a different Hf:Zr ratio. Moreover, the observed increasing monoclinic phase fraction with increasing annealing temperature could not be explained.[33] This points to the conclusion that not only thermodynamics, but also kinetic effects, need to be considered to explain the physical origin of the formation of the orthorhombic phase.[33]

Although not all controlling parameters are understood in detail, it is now established that ferroelectricity can be reproducibly achieved in thin hafnium oxide-based films in the thickness range of 5–30 nm, thus it is suitable for further device development. As shown in **Table I**, ferroelectric hafnium oxide doped with various dopants has one order of magnitude higher E_c and similar polarization compared to ferroelectric perovskites. E_c is even higher than that of the polymer ferroelectric poly(vinylidene fluoride). Additionally, the permittivity is much lower than in perovskites, which is an important aspect in reducing the depolarization field in the FeFET.

FeRAMs

The most straightforward way to realize a ferroelectric memory is to use the DRAM architecture, replacing the dielectric by a ferroelectric and pulsing the plate line instead of keeping it grounded (see Figure 2a). This modification is necessary since in the ferroelectric capacitor, compared to DRAM where the electrical field is supplied by the charged capacitor, the storage is maintained at 0 V and the capacitor needs to be actively driven via the plate line to read the stored polarization (see Figure 1d). To increase the signal, in the early days, two such cells, where one is written into the direction that should be stored (e.g., 0) and the other is written into the opposite direction (e.g., 1), were combined to realize one bit. Later, the second cell was replaced by one reference cell for a large number of cells in order to save space. The first products appeared on the

https://doi.org/10.1557/mrs.2018.92

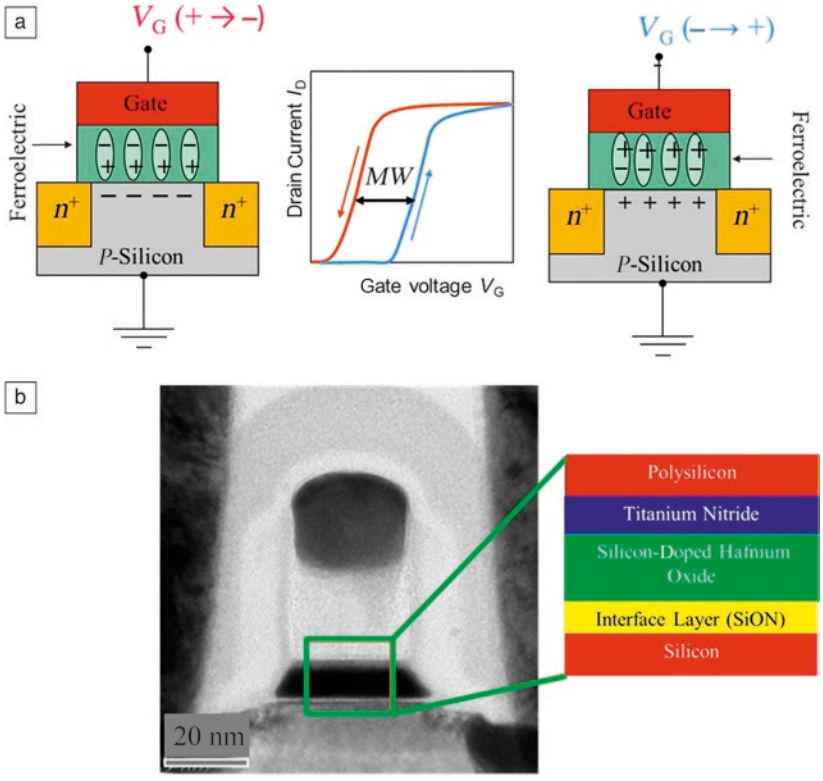


Figure 3. Ferroelectric field-effect transistor (FeFET) as (a) a concept and (b) transmission electron microscope micrograph of the FeFET cross section realized in a 28-nm complementary metal oxide semiconductor process. The different layers in the gate stack are indicated on the right.[53] Note: *MW*, memory window.

market as early as 1993,[5] and today, advanced products use 130-nm technology.[10] However, further success beyond niche markets is hindered by the fact that a 3D capacitor has not been practically realized using perovskite materials.[8,9]

With ferroelectric hafnium oxide, the full advantages of 3D integration can be attained[34] (see Figure 2b). However, now, the high coercive field of ferroelectric hafnium oxide is the limiting factor. On the one hand, device operation at low operating voltages is challenging. On the other hand, field cycling uses fields close to the breakdown value, limiting the device endurance with respect to the number of possible switching cycles.[35] Note that due to the destructive read in the FeRAM concept, read cycles also contribute to the total number of endurance cycles. Moreover, effects like wakeup (increase in remanent polarization during the early stages of cycling) and fatigue (reduction in remanent polarization for high cycle numbers) still need to be engineered to levels as those found in perovskite ferroelectrics.[36,37] The issue of operating at low supply voltage can be tackled by engineering the coercive field. To date, the fabrication parameters have been observed to have only weak influence on the coercive field. An oxide thickness as low as 5 nm was fabricated with good electrical parameters.[38] Attempts at further lowering the thickness were also made,[39] although it is challenging to verify the ferroelectricity in the case that leakage becomes dominant.[40]

Our understanding of endurance has also significantly progressed in the last three to four years,[41] though much can still be learned from the optimization of lead zirconium titanate.[42] Recently, another approach has been proposed to increase the endurance in the 1-transistor-1-capacitor (1T-1C) architecture. When stabilizing ferroelectricity in hafnium oxide by dopants with radius smaller than that of Hf and at doping concentrations higher than the optimum to achieve ferroelectricity, a pinched or antiferroelectric hysteresis is observed.[17,24,26,31] (see Figure 2c; dotted line). Specifically, in the hafnium-zirconium-oxide system, this behavior is even observed for pure zirconium oxide.[43] The cycling endurance for such a structure is much higher compared to that of the ferroelectric case.[44] However, since there is no remanent polarization, P_R, when the electrical field is removed, the system is not nonvolatile. Pesic et al. proposed the use of a bias field that can be generated by either electrodes with different work-function values[44,45] or additional fixed charges or dipoles placed inside the dielectric stack.[46] They verified this possibility using capacitor test structures.[44–46] The advantage of this approach is that now the cycling is performed between a polarized and an unpolarized state. As a result, the apparent coercive field is cut in half, and the endurance is drastically improved. Antiferroelectric hysteresis was also observed in dielectric stacks similar to those used in state-of-the-art DRAM capacitors,[45] making this a possible extension of today's DRAM technology toward a nonvolatile RAM memory.[47] Thus, ferroelectric hafnium oxide can overcome the scaling limitation of FeRAMs since mature atomic layer deposition processes exist that allow deposition of material on high-aspect-ratio capacitors. However, the higher E_c imposes additional challenges. Material engineering or an alternative approach

Table I. Comparison of coercive field, E_c, and switched polarization charge, $2P_R$, for strontium bismuth tantalate (SBT), lead zirconium titanate (PZT), poly(vinylidene fluoride):tetrafluoroethylene (PVDF-TRFE), and doped hafnium oxide.

	SBT ($Sr_2Bi_2TaO_9$)	PZT	PVDF-TRFE	Doped HfO_2
Coercive field E_c in MV/cm	0.05	0.1	0.5	0.8–2
Switched charge ($2P_R$) in μC/cm²	15–25	30–60	10	30–60

The values given for the doped hafnium oxide span the range that have been observed using different dopants such as Si, Al, Y, La, as well as mixed crystals from Hf and Zr.

using the antiferroelectric hysteresis are possible options to overcome these limitations. To date, no fully integrated 1T-1C FeRAM array structures have been reported and research has been mainly carried out on capacitor test structures.

FeFETs

The main issues of a 1T-1C memory cell can be overcome if the ferroelectric is integrated into the gate stack of a FeFET (Figure 3a), as explained in the Introduction section.[11] Assuming an *n*-channel transistor and high enough polarization that if oriented in a way that the negative charge is close to the channel and the positive charge is close to the gate electrode, the channel will be in accumulation mode. We can also assume that if the polarization is the other way around, then the channel will be in the inversion condition. If we start in the OFF state and the gate voltage is swept to a point where the positive coercive field of the ferroelectric is reached and finally exceeded, the channel will turn on. When sweeping back beyond the point where the negative coercive field is reached, the channel will be switched OFF again. Therefore, if the positive coercive field E_{c+} and negative coercive field E_{c-} (see Figure 1c) have the same absolute value E_c, the memory window (*MW*) (the difference between the two threshold voltages of the device for the two different polarization states) is given by the difference between the voltages where the respective coercive fields are reached:[48]

$$MW = 2 \cdot E_c \cdot d_{Fe}. \quad (1)$$

Here, d_{Fe} is the thickness of the ferroelectric film.

It should be noted that Equation (1) was deduced using a simplified picture. In practice, deviations from the previously discussed assumptions and the depolarization fields discussed later need to be considered. However, the consequence that the maximum attainable memory window is limited by the coercive field holds true and is important. Hence, the high coercive field of hafnium oxide ferroelectrics is actually a benefit rather than a drawback.

Using perovskites, much thicker ferroelectric films would be needed to achieve the same memory window, which limits scalability. Only for remanent polarization of the ferroelectric that is too low to cause sufficient electrical field can we expect a significant influence of the remanent polarization on the memory window.[48] Eventually, the remanent polarization will influence the effective gate overdrive of the device, and therefore, will influence the ON current.[48] Because of threshold voltage shifts during polarization switching, a lower subthreshold swing, compared to a nonferroelectric transistor that has the same effective gate dielectric thickness, can be achieved. The subthreshold swing is the voltage swing that is required to change the transistor current by one order of magnitude and describes the ability to efficiently switch the transistor between the ON and OFF states. However, if the effect is not a consequence of a stabilized negative capacitance effect,[49] the polarization reversal would lead to a switching hysteresis.

In the transistor, a serial capacitor consisting of not only the capacitance of the depletion layer in the semiconductor, but also the unavoidable interface oxide between the channel and the ferroelectric, is an integral part of the structure. This series connection means the voltage that has to be applied to the device for polarization switching is increased compared to the case of a pure ferroelectric capacitor, and in the case of no applied electrical field (e.g., the case of retention), an increased internal depolarization field will be the consequence.[12] Since perovskite-based ferroelectrics have permittivity in the range of a few hundreds, a large thickness is required to balance this inherent capacitive divider. The much lower permittivity of hafnium oxide is beneficial here, and additionally, the high coercive field helps to stabilize the polarization in the retention case.[50] Therefore, hafnium-based ferroelectrics seem to be favorable to realize FeFETs.

The first demonstrations occurred in 2011.[51,52] In 2012, it was verified that use of ferroelectric hafnium oxide can close the scaling gap between FeFETs and conventional FETs.[53] Encouraged by this work, in 2016, the first fully integrated technology, where FeFET memory arrays were embedded in a 28-nm CMOS process, was demonstrated[54] (Figure 3b). One year later, scaling to 22-nm fully depleted silicon-on-insulator technology together with further advances in the performance of the memory arrays were shown.[55]

Thus, the vision of realizing nonvolatile memories based on FeFETs has moved to realization much faster than in the previous 30 years of research. However, memories are not the only application for FeFETs. Salahuddin and Datta[49] proposed the concept of negative capacitance transistors in 2008 to overcome the so-called Boltzmann tyranny. This means that the subthreshold slope of FETs are limited to 60 mV/decade at room temperature, therefore, scaling of the supply voltage is limited. This concept makes use of stabilizing the ferroelectric in the negative differential capacitance region between the two stable polarization states by using a suitable dielectric capacitor in series. The negative differential capacitance region is caused by an energy barrier giving rise to a negative change in charge with changing voltage (see Figure 1b). Eventually, the stabilized negative capacitance will lead to a voltage boost on the internal node between the ferroelectric and the transistor dielectric. Consequently, a smaller subthreshold swing together with a higher ON current is possible.[56]

Again, the integration challenge of combining ferroelectrics with CMOS processes needs to be overcome and ferroelectric hafnium oxide seems to be the material of choice for such devices. Initial device demonstrations have been shown,[57,58] although the issue of stabilization of the negative capacitance state remains to be resolved. As a first step, the transient negative capacitance was observed.[59] However, the exact boundary conditions for stabilizing the negative capacitance operation region are still under scientific debate and need clarification.[60–62]

Summary and future prospects

From a physical viewpoint, ferroelectrics are an almost ideal candidate for binary nonvolatile memories, since they have a

https://doi.org/10.1557/mrs.2018.92

field-driven switching mechanism. However, the complexity of the traditional perovskite materials and the resulting difficulties to integrate them into the CMOS process has hindered the fast scaling of such devices. The unexpected discovery of ferroelectricity in doped hafnium oxide has completely changed this picture, because hafnium oxide is a standard material in CMOS processing, with manufacturing processes available for different scenarios.

From an electrical parameter point of view, ferroelectric hafnium oxide differs from perovskites in having a much higher coercive field, E_c, and a much lower permittivity. When using the material in the traditional 1T-1C ferroelectric RAM configuration, the high coercive field imposes challenges with respect to low-voltage operation and cycling endurance. Antiferroelectric memory has been proposed to overcome these limitations. When integrating ferroelectric hafnium oxide into the gate stack of a transistor, resulting in a FeFET, both aspects give this material a competitive edge. The developmental progress of FeFETs has significantly increased by the adoption of ferroelectric hafnium oxide.

Nevertheless, achieving a cycling endurance beyond the level of conventional charge-based nonvolatile memories remains a challenge.[39,63] Different strategies have been proposed to overcome these limitations[64] and encouraging results have recently been published.[65] The fact that differently optimized FeFETs are also an option to make steep subthreshold devices by stabilizing the negative capacitance region has further inspired the research and development of such devices. Finally, ferroelectricity is a material property that is accompanied by piezoelectricity and pyroelectricity.[1,20,22] These properties open the path toward integrated sensors, actuators, and energy-harvesting functionalities, and these are only in the early stages of exploration.[21,66,67]

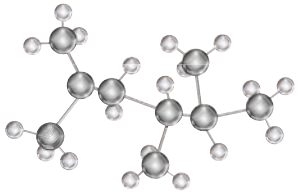
Acknowledgments

The authors thank all current and former team members at NaMLab, Fraunhofer IPMS-CNT, Global Foundries, Seoul National University, and all cooperation partners for their dedicated work on ferroelectric hafnium oxide and its applications. Part of this work was supported by the EFRE Fund of the European Commission within the scope of technology development, the Free State of Saxony (Germany), and the German Research Foundation (Deutsche Forschungsgemeinschaft; Project MI 1247/11–2). M.H.P. is supported by a Humboldt Postdoctoral Fellowship from the Alexander von Humboldt Foundation.

References

1. T. Mitsui, "Ferroelectrics and Antiferroelectrics," in *Springer Handbook of Condensed Matter and Materials Data*, W. Martienssen, H. Warlimont, Eds. (Springer-Verlag Berlin, 2005), pp. 903–938.
2. T. Mikolajick, C.-U. Pinnow, *Proc. Nonvolatile Mem. Technol. Symp.* (JPL Publishing, Pasadena, CA, 2002), pp. 4–6.
3. D.A. Buck, "Ferroelectrics for Digital Information Storage and Switching," master's thesis, Massachusetts Institute of Technology Digital Computer Laboratory (1952).
4. J.R. Anderson, *Trans. Am. Inst. Electr. Eng. Pt.* 1 **71**, 395 (1953).
5. D. Bondurant, *Ferroelectrics* **112**, 273 (1990).
6. C.-U. Pinnow, T. Mikolajick, *J. Electrochem. Soc.* **151**, K13 (2004).
7. S.Y. Lee, K. Kim, *Int. Electron Devices Mtg.* (2002), pp. 547–550.
8. J.-M. Koo, B.-S. Seo, S. Kim, S. Shin, J.-H. Lee, H. Baik, J.-H. Lee, J.H. Lee, B.-J. Bae, J.-E. Lim, D.-C. Yoo, S.-O. Park, H.-S. Kim, H. Han, S. Baik, J.-Y. Choi, Y.J. Park, Y. Park, *Int. Electron Devices Mtg.* (2005), pp. 340–343.
9. C.-P. Yeh, M. Lisker, B. Kalkofen, E.P. Burte, *AIP Adv.* **6** (3), 035128 (2016).
10. H.P. McAdams, R. Acklin, T. Blake, X.-H. Du, J. Eliason, J. Fong, W.F. Kraus, D. Liu, S. Madan, T. Moise, S. Natarajan, N. Qian, Y. Qiu, K.A. Remack, J. Rodriguez, J. Roscher, A. Seshadri, S.R. Summerfelt, *IEEE J. Solid-State Circuits* **39**, 667 (2004).
11. I.M. Ross, "Semiconductive Translating Device," US Patent US2791760 A (1955).
12. T.P. Ma, J.-P. Han, *IEEE Electron Device Lett.* **23**, 386 (2002).
13. S. Sakai, R. Ilangovan, *IEEE Electron Device Lett.* **25**, 369 (2004).
14. J. Robertson, *Eur. J. Appl. Phys.* **28**, 265 (2004).
15. M.T. Bohr, R.S. Chau, T. Ghani, K. Mistry, *IEEE Spectr.* **44**, 29 (2007).
16. R. Materlik, C. Künneth, A. Kersch, *J. Appl. Phys.* **117**, 134109 (2015).
17. T.S. Böscke, J. Müller, D. Bräuhaus, U. Schröder, U. Böttger, *Appl. Phys. Lett.* **99**, 102903 (2011).
18. T.S. Böscke, St. Teichert, D. Bräuhaus, J. Müller, U. Schröder, U. Böttger, T. Mikolajick, *Appl. Phys. Lett.* **99**, 112904 (2011).
19. J.F. Scott, *J. Phys. Condens. Matter* **20** (2), 021001 (2007), http://iopscience.iop.org/article/10.1088/0953-8984/20/02/021001/meta.
20. D. Martin, J. Müller, T. Schenk, T.M. Arruda, A. Kumar, E. Strelcov, E. Yurchuk, S. Müller, D. Pohl, U. Schröder, S.V. Kalinin, T. Mikolajick, *Adv. Mater.* **26**, 8198 (2014).
21. M. Hoffmann, U. Schroeder, C. Künneth, A. Kersch, S. Starschich, U. Böttger, T. Mikolajick, *Nano Energy* **18**, 154 (2015).
22. S.W. Smith, A.R. Kitahara, M.A. Rodriguez, M.D. Henry, M.T. Brumbach, J.F. Ihlefeld, *Appl. Phys. Lett.* **110**, 072901 (2017).
23. J. Mueller, U. Schröder, T.S. Böscke, I. Müller, U. Böttger, L. Wilde, J. Sundqvist, M. Lemberger, P. Kücher, T. Mikolajick, L. Frey, *J. Appl. Phys.* **110**, 114113 (2011).
24. S. Mueller, J. Mueller, A. Singh, S. Riedel, J. Sundqvist, U. Schroeder, T. Mikolajick, *Adv. Funct. Mater.* **22**, 2412 (2012).
25. J. Müller, T.S. Böscke, D. Bräuhaus, U. Schröder, U. Böttger, J. Sundqvist, P. Kücher, T. Mikolajick, L. Frey, *Appl. Phys. Lett.* **99**, 112901 (2011).
26. U. Schroeder, E. Yurchuk, J. Müller, D. Martin., T. Schenk, P. Polakowski, C. Adelmann, M.I. Popovici, S.V. Kalinin, T. Mikolajick, *Jpn. J. Appl. Phys.* **53**, 08LE02 (2014).
27. L. Xu, S. Shibayama, K. Izukashi, T. Nishimura, T. Yajima, S. Migita, A. Toriumi, *IEEE Int. Electron Devices Mtg.* (2016), pp. 25.2.1–25.2.4.
28. P. Polakowski, J. Müller, *Appl. Phys. Lett.* **106**, 232905 (2015).
29. X. Sang, E.D. Grimley, T. Schenk, U. Schroeder, J.M. LeBeau, *Appl. Phys. Lett.* **106**, 162905 (2015).
30. M.H. Park, T. Schenk, C.M. Fancher, E.D. Grimley, C. Zhou, C. Richter, J.M. LeBeau, J.L. Jones, T. Mikolajick, U. Schroeder, *J. Mater. Chem. C* **5**, 4677 (2017).
31. E. Yurchuk, J. Müller, S. Knebel, J. Sundqvist, A.P. Graham, T. Melde, U. Schröder, T. Mikolajick, *Thin Solid Films* **533**, 88 (2013).
32. M.H. Park, Y.H. Lee, H.J. Kim, T. Schenk, W. Lee, K.D. Kim, F.P.G. Fengler, T. Mikolajick, U. Schroeder, C.S. Hwang, *Nanoscale* **9**, 9973 (2017).
33. M.H. Park, H.J. Kim, T. Moon, K.D. Kim, Y.H. Lee, S.D. Hyun, T. Mikolajick, U. Schroeder, C.S. Hwang, *Nanoscale* **10**, 716 (2018).
34. P. Polakowski, S. Riedel, W. Weinreich, M. Rudolf, J. Sundqvist, K. Seidel, J. Müller, *2014 Int. Mem. Workshop* (2014), pp. 1–4.
35. E. Yurchuk, S. Mueller, D. Martin, S. Slesazeck, U. Schroeder, T. Mikolajick, J. Müller, J. Paul, R. Hoffmann, J. Sundqvist, T. Schlosser, R. Boschke, R. van Bentum, M. Trentzsch, *Reliability Physics Symp. 2014 IEEE Int.* (2014) pp.2E.5.1–2E.5.5.
36. T. Schenk, M. Hoffmann, J. Ocker, M. Pešić, T. Mikolajick, U. Schroeder, *ACS Appl. Mater. Interfaces* **7**, 20224 (2015).
37. M. Pešić, F.P.G. Fengler, L. Larcher, A. Padovani, T. Schenk, E.D. Grimley, X. Sang, J.M. LeBeau, S. Slesazeck, U. Schroeder, T. Mikolajick, *Adv. Funct. Mater.* **26**, 4601 (2016).
38. J. Müller, P. Polakowski, S. Mueller, T. Mikolajick, *ECS J. Solid State Sci. Technol.* **4** (5), N30 (2015).
39. A. Chernikova, M. Kozodaev, A. Markeev, D. Negrov, M. Spiridonov, S. Zarubin, O. Bak, P. Buragohain, H. Lu, E. Suvorova, A. Gruverman, A. Zenkevich, *ACS Appl. Mater. Interfaces* **8**, 7232 (2016).
40. T. Schenk, U. Schroeder, T. Mikolajick, *IEEE Trans. Ultrason. Ferroelectr. Freq. Control* **62** (3), 596 (2015)
41. U. Schroeder, M. Pešic, T. Schenk, H. Mulaosmanovic, S. Slesazeck, J. Ocker, C. Richter, E. Yurchuk, K. Khullar, J. Müller, P. Polakowski, E.D. Grimley, J.M. LeBeau, S. Flachowsky, S. Jansen, S. Kolodinski, R. van Bentum, A. Kersch, C. Künneth, T. Mikolajick, *Eur. Solid-State Device Res. Conf.* (2016), pp. 364–368.
42. F.P.G. Fengler, M. Pešić, S. Starschich, T. Schneller, C. Künneth, U. Böttger, H. Mulaosmanovic, T. Schenk, M.H. Park, R. Nigon, P. Muralt, T. Mikolajick, U. Schroeder, *Adv. Electron. Mater.* **3**, 1600505 (2017).

43. J. Müller, T.S. Böscke, U. Schröder, S. Mueller, D. Bräuhaus, U. Böttger, L. Frey, T. Mikolajick, *Nano Lett.* **12**, 4318 (2012).
44. M. Pešić, S. Knebel, M. Hoffmann, C. Richter, T. Mikolajick, U. Schroeder, *IEEE Int. Electron Devices Mtg.* (2016), pp. 11.6.1–11.6.4.
45. M. Pešić, M. Hoffmann, C. Richter, T. Mikolajick, U. Schroeder, *Adv. Funct. Mater.* **26**, 7486 (2016).
46. M. Pešić, M. Hoffmann, C. Richter, S. Slesazeck, T. Kämpfe, L.M. Eng, T. Mikolajick, U. Schroeder, *Eur. Solid-State Device Res. Conf.* 160 (2017).
47. M. Pešić, M. Hoffmann, C. Richter, S. Slesazeck, U. Schroeder, T. Mikolajick, *Proc. Nonvolatile Mem. Technol. Symp.* (2017), doi: 10.1109/NVMTS.2017.8171307.
48. S.L. Miller, P.J. McWhorter, *J. Appl. Phys.* **72**, 5999 (1992).
49. S. Salahuddin, S. Datta, *Nano Lett.* **8**, 405 (2008).
50. N. Gong, T.P. Ma, *IEEE Electron Device Lett.* **37**, 1123 (2016).
51. T.S. Böscke, J. Müller, D. Bräuhaus, U. Schröder, U. Böttger, *Int. Electron Devices Mtg.* (2011), pp. 24.5.1–24.5.4.
52. J. Müller, T.S. Boescke, U. Schroder, R. Hoffmann, T. Mikolajick, L. Frey, *IEEE Electron Device Lett.* **33** (2), 185 (2012).
53. J. Müller, E. Yurchuk, T. Schlösser, J. Paul, R. Hoffmann, S. Müller, D. Martin, S. Slesazeck, P. Polakowski, J. Sundqvist, M. Czernohorsky, K. Seidel, P. Kücher, R. Boschke, M. Trentzsch, K. Gebauer, U. Schröder, T. Mikolajick, *Symp. VLSI Technol. Dig. Tech. Pap.* (2012), p. 25.
54. M. Trentzsch, S. Flachowsky, R. Richter, J. Paul, B. Reimer, D. Utess, S. Jansen, H. Mulaosmanovic, S. Müller, S. Slesazeck, J. Ocker, M. Noack, J. Müller, P. Polakowski, J. Schreiter, S. Beyer, T. Mikolajick, B. Rice, *IEEE Int. Electron Devices Mtg.* (2016), pp. 11.5.1–11.5.4.
55. S. Duenkel, M. Trentzsch, R. Richter, P. Moll, C. Fuchs, O. Gehring, M. Majer, S. Wittek, B. Müller, T. Melde, H. Mulaosmanovic, S. Slesazeck, S. Müller, J. Ocker, M. Noack, D.-A. Löhr, P. Polakowski, J. Müller, T. Mikolajick, J. Höntschel, B. Rice, J. Pellerin, S. Beyer, *IEEE Int. Electron Devices Mtg.* (2017), pp. 19.7.1–19.7.4.
56. C.I. Lin, A.I. Khan, S. Salahuddin, C. Hu, *IEEE Trans. Electron Devices* **63** (5), 2197 (2016).
57. K.S. Li, P.-G. Chen, T.-Y. Lai, C.-H. Lin, C.-C. Cheng, C.-C. Chen, Y.-J. Wei, Y.-F. Hou, M.-H. Liao, M.-H. Lee, M.-C. Chen, J.-M. Sheih, W.-K. Yeh, F.-L. Yang, S. Salahuddin, C. Hu, *IEEE Int. Electron Devices Mtg.* (2015), pp. 22.6.1–22.6.4.
58. M.H. Lee, S.-T. Fan, C.-H. Tang, Y.-C. Chou, H.-H. Chen, J.-Y. Kuo, M.-J. Xie, S.-N. Liu, M.-H. Liao, C.-A. Jong, K.-S. Li, M.-C. Chen, C.W. Liu, *IEEE Int. Electron Devices Mtg.* (2016), pp. 12.1.1–12.1.4.
59. M. Hoffmann, M. Pešić, K. Chatterjee, A.I. Khan, S. Salahuddin, S. Slesazeck, U. Schroeder, T. Mikolajick, *Adv. Funct. Mater.* **20**, 8643 (2016).
60. M. Hoffmann, M. Pešić, S. Slesazeck, U. Schroeder, T. Mikolajick, *Joint Int. EUROSOI Workshop Int. Conf. Ultimate Integration Silicon (EUROSOI-ULIS)* (2017), pp. 1–4.
61. Y.J. Kim, M.H. Park, Y.H. Lee, H.J. Kim, W. Jeon, T. Moon, K.D. Kim, D.S. Jeong, H. Yamada, C.S. Hwang, *Sci. Rep.* **6**, 19039 (2016).
62. Y.J. Kim, H. Yamada, T. Moon, Y.J. Kwon, C.H. An, H.J. Kim, K.D. Kim, Y.H. Lee, S.D. Hyun, M.H. Park, C.S. Hwang, *Nano Lett.* **16** (7), 4375 (2016).
63. E. Yurchuk, J. Müller, S. Müller, J. Paul, M. Pešić, R. van Bentum, U. Schroeder, T. Mikolajick, *IEEE Trans. Electron Devices* **63** (9), 3501 (2016).
64. J. Mueller, P. Polakowski, S. Muller, H. Mulaosmanovic, J. Ocker, T. Mikolajick, S. Slesazeck, S. Flachowsky, M. Trentzsch, *Non-Volatile Mem. Technol. Symp.* (Pittsburgh, PA, 2016), pp. 1–7.
65. K. Chatterjee, S. Kim, G. Karbasian, A.J. Tan, A.K. Yadav, A.I. Khan, C. Hu, S. Salahuddin, *IEEE Electron Device Lett.* **38** (10), 1379 (2017).
66. M.H. Park, H.J. Kim, Y.J. Kim, T. Moon, K.D. Kim, C.S. Hwang, *Nano Energy* **12**, 131 (2015).
67. M.H. Park, T. Schenk, M. Hoffmann, S. Knebel, J. Gärtner, T. Mikolajick, U. Schroeder, *Nano Energy* **36**, 381 (2017).
68. J. Müller, T.S. Böscke, S. Müller, E. Yurchuk, P. Polakowski, J. Paul, D. Martin, T. Schenk, K. Khullar, A. Kersch, W. Weinreich, S. Riedel, K. Seidel, A. Kumar, T.M. Arruda, S.V. Kalinin, T. Schlösser, R. Boschke, R. van Bentum, U. Schröder, T. Mikolajick, *IEEE Int. Electron Devices Mtg.* (Washington, DC, 2013), pp. 10.8.1–10.8.4. □



Thomas Mikolajick has been a professor of nanoelectronic materials at Technische Universität Dresden (TU Dresden) and a scientific director of the Nanoelectronic Materials Laboratory gGmbH, Germany, since 2009. He received his Dipl-Ing degree in 1990 and his Dr-Ing degree in 1996 in electrical engineering, both from the Friedrich-Alexander-Universität Erlangen-Nürnberg, Germany. From 1996 to 2006, he worked in the semiconductor industry at Siemens, Infineon and Qimonda. In 2006, he was appointed professor of materials science of electron devices at Technische Universität Bergakademie Freiberg, Germany. Since 2009, he holds a professorship for nanoelectronic materials at TU Dresden in combination with the position of scientific director of the Nanoelectronic Materials Lab. He has authored or co-authored more than 300 publications and holds approximately 50 patents. Mikolajick can be reached by email at thomas.mikolajick@namlab.com.

Stefan Slesazeck joined the Nanoelectronic Materials Laboratory gGmbH, Germany, as senior scientist in 2009. He received his PhD degree in microelectronics from Technische Universität Dresden, Germany, in 2004. He joined Qimonda Dresden as a device engineer and studied the predevelopment of three-dimensional dynamic random-access memories (DRAMs) down to 46-nm technology and concept evaluation for 1T-DRAM. His current interests include device and concept development, electrical characterization, and modeling of memories. He is the author/co-author on more than 80 papers and holds six US patents. Slesazeck can be reached by email at stefan.slesazeck@namlab.com.

Min Hyuk Park has been a postdoctoral researcher in the Nanoelectronic Materials Laboratory gGmbH, Germany, since 2015. He received his BS degree in 2008, and his MS and PhD degrees in 2014, both in materials science and engineering from Seoul National University, South Korea. He has been supported by the Alexander von Humboldt Foundation since 2016. His research interests include ferroelectric and antiferroelectric (Hf, Zr)O_2 and doped HfO_2 thin films for memory, energy storage, energy harvesting, solid-state cooling, and sensor applications. He has co-authored more than 40 papers. Park can be reached by email at minhyuk.park@namlab.com.

Uwe Schroeder joined the Nanoelectronic Materials Laboratory gGmbH, Germany, in 2009. He received his PhD degree from the University of Bonn, Germany, in 1995, and subsequently, he was a postdoctoral researcher at The University of Chicago. In 1997, he joined Infineon, formerly Siemens Semiconductor, for dynamic random-access memories (DRAMs) capacitor development in the DRAM Development Alliance with IBM and Toshiba, before transferring to Infineon's Memory Development Center, Germany, in 2000. His current research focuses on high-*k* dielectrics and ferroelectric HfO_2 layers in semiconductor devices. He has co-authored more than 150 papers and conference contributions and holds more than 30 patents. Schroeder can be reached by email at uwe.schroeder@namlab.com.